

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Li

Docket No.:

2003 P 54309 US

Serial No.:

10/748,995

Art Unit:

TBD

Filed:

December 30, 2003

Examiner:

TBD

For:

Transistor with Silicon and Carbon Layer in the Channel Region

Certificate of Mailing via First Class Mail (37 C.F.R. § 1.8(a))

Date of Deposit:

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Certificate of Mailing via First Class Mail (1 page) Information Disclosure Statement (1 page) Form PTO/SB/08A (1 page) with one reference attached Return Postcards (2)

Respectfully submitted,

Dusty Dudley

Legal Assistant

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INFORMATION DISCLOSURE STATEMENT

Dear Sir:

The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(1), within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d).

February 5, 2004

Date

Respectfully submitted,

Kay Houston

Attorney for Applicant

Reg. No. 38,495

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PTO/SB/08A (05-03)
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Substitute for form 1449A/PTO				Complete if Known		
				Application Number	10/748,995	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	December 30, 2003	
				First Named Inventor	Li	
				Art Unit	TBD	
(use as many sheets as necessary)				Examiner Name	ТВО	
Sheet	1	of	1	Attorney Docket Number	2003 P 54309 US	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.1	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
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FOREIGN PATENT DOCUMENTS						
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OTHER PRIOR ART NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	.T ²		
	1	"Front End Processes," International Technology Roadmap for Semiconductor (ITRS), 2003 Edition, pp. 23–25, http://member.itrs.net/.			

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Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.